Multi-Channel Transcutaneous Cortical Stimulation System

Contract # N01-NS-7-2365

Progress Report #9

for the contract period 4/31/99 – 7/30/99

Illinois Institute of Technology

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Introduction

The goal of this project is the design, fabrication, and testing of a ***Multi-Channel Transcutaneous Cortical Stimulation System*** to be used in a prototype artificial vision system**.** During the past 25 years, the development of a neuroprosthesis that could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This project uses the combined capability four organizations, the Illinois Institute of Technology, BioElectric Inc., Cross Technology, and the A.E. Mann Foundation to accomplish this challenging task.

This is the ninth progress report for this project. In this report we describe our progress on defining fabrication methods for the hermetic seals, fundamental tests of the glass to ceramic seals and our progress on the ASIC designs.

Progress on Design of the Implant Package

In our eighth progress report we reported that we had met with Electrofilms in order to define the fabrication steps for the metallized ceramic substrates to be used for the first and second layers of the hermetic package. We had hoped to obtain prototype substrates for testing with the glass seals. However, fabrication delays at Electrofilms prevented delivery of these first substrates. We have proceeded with the analytical testing of the glass seals and fabricated sealed ceramic packages which are now ready for helium leak testing.

We have also met with BioElectric to increase their level of involvement in the fabrication of the connectors.

Fabrication

By way of review, in Figure 1, we show the location of one of the glass-to-ceramic seals between ceramic layer #2 and ceramic layer #3. The seal is formed by depositing the glass, in the green state, on layer #2 via a syringe controlled by the X-Y-Z table. The green glass is dried at 100ºC – 150ºC in a convection oven. Layers #2 and #3 are pressed together, then fired in a furnace using a ramped temperature profile at a maximum of 385ºC.

This quarter we have fabricated sealed ceramic modules consisting of two layers of 0.08" thick ceramic. In our implant package design, the ceramic layers will be 0.015" thick. We have used the thicker ceramic for two reasons: first, the thicker ceramic is less expensive and readily available. We have obtained a large supply of these thick sheets. Second, use of the thicker ceramic material temporarily avoids the issue of how the ceramic sheet is held down in the numerical-controlled milling machine. For these thicker sheets, a conventional clamping system can be used. For the thinner sheets an adhesive-based hold-down method is being developed.

Gross leak testing of the thick ceramic modules has been successful. In all of our samples, we have found no detectable leaks. We are presently preparing more of these thick modules for more sensitive helium leak testing at the Mann Foundation. In addition to these thick ceramic

modules we have also fabricated more samples of the ceramic/glass modules. These hybrid modules seal a sheet of glass to a ceramic sheet. A cavity machined into the ceramic sheet simulates the cavity of the all-ceramic electronic submodule. The hybrid modules are convenient because they permit visual examination of the seal region through the glass sheet. We have placed samples of these hybrid modules in our 90° C. saline tank. Visual examination of the module's interior can reveal condensed moisture, indicating a leak. Examination of the seal can also reveal corrosion of the glass.

Earlier samples made from two sheets of glass have been on test for approximately 1 year. And hybrid packages have been on test for approximately 3 months. None of the samples show any signs of seal corrosion or moisture condensation. Failure of the packages is invariably due to fracturing of the glass sheet, most likely due to a thermal mismatch between the glass and the ceramic. During the next two quarters we plan to intensity our testing efforts using all-ceramic packages.

In addition to the hot saline tests, we have also used the thicker ceramic modules to investigate the feasibility of polishing the connector edges. Using standard laboratory equipment, at IIT, we have successfully polished the edges of the sealed modules. Presently we are designing a fixture to hold the more delicate thin ceramic modules.

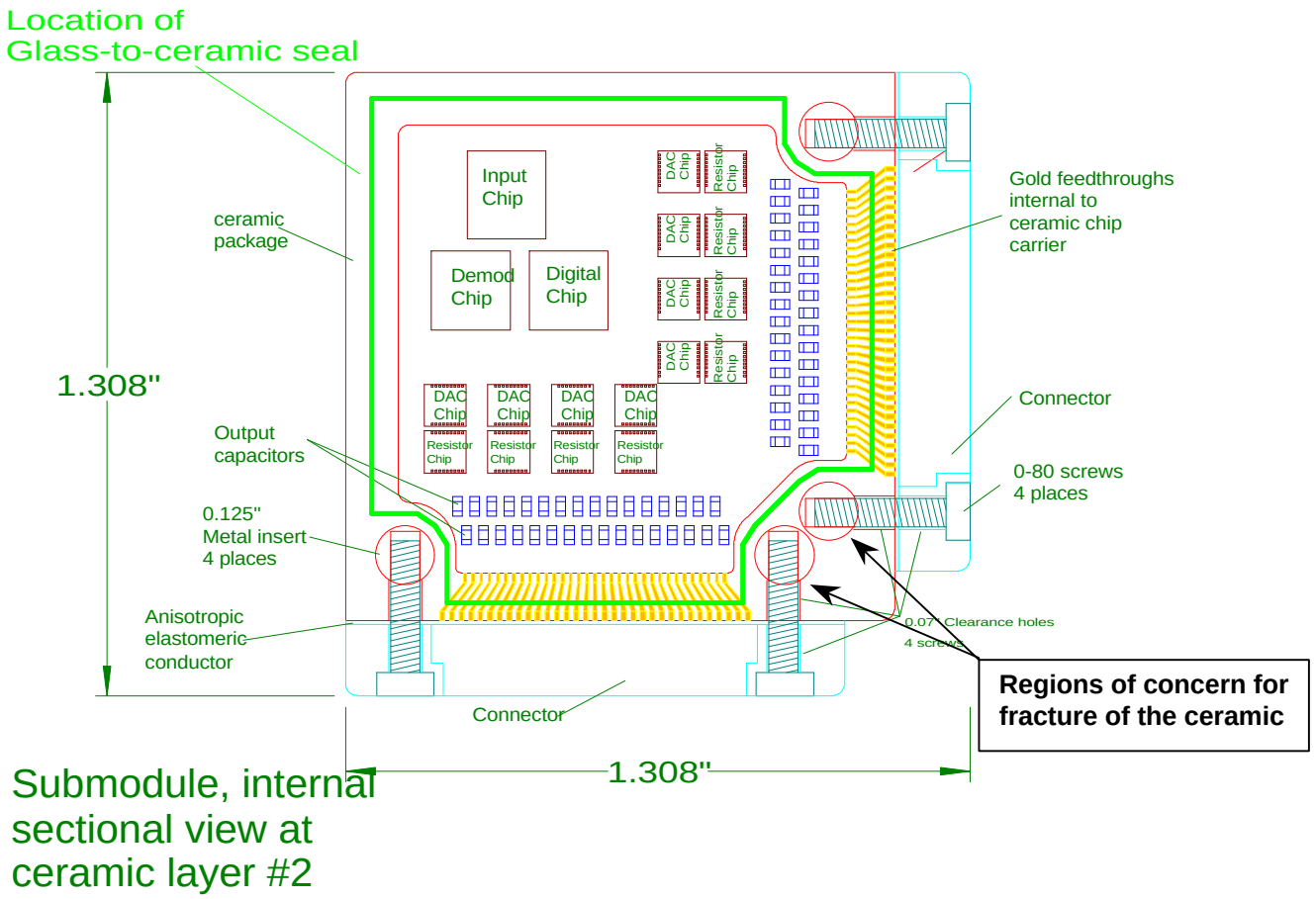


Figure 1 – Submodule section at layer #2 showing location of the glass seal.

Connector Design and Testing

Our connector design is based upon the pressure-seal principle using an anisotropic elastomeric membrane for electrical contact. In order for this approach to be successful, approximately 300 PSI must be applied to the anisotropic elastomer. In our design, this accomplished by tightening the connector screws to a specified torque.

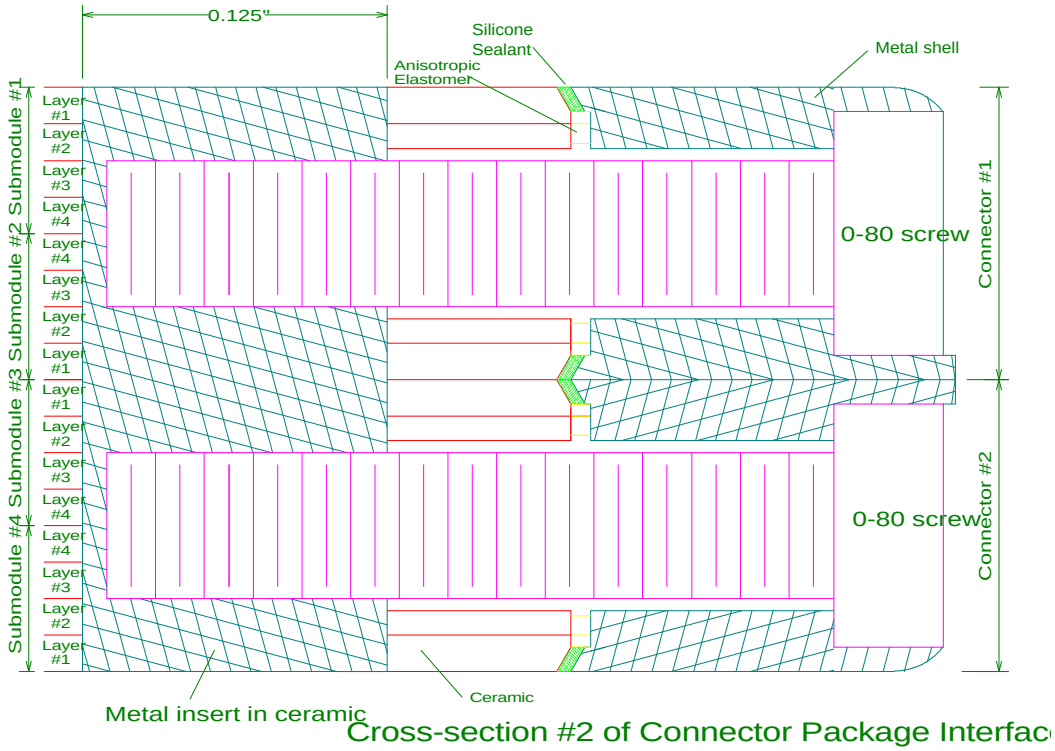


Figure 2 – Cross-section of the ceramic package at the location of the connector screws.

We have been concerned about the stress at the location of the connector posts, as the connector is tightened against the ceramic edge. Computations, performed at BioElectric, predict that the two connector screws need to be tightened to a torque of 4-6 in-oz. in order to produce the required 300 PSI.

Therefore we fabricated a mock-up of the two ceramic submodules, complete with screw access holes, and anisotropic membrane, so that we could test the tightening of the screws to the specified torque. Our first sample allowed for a maximum torque of approximately 4 in-oz. prior to fracturing of the ceramic. The location and shape of the fracture line was consistent with a highly localized stress a the interface of the post and ceramic. Microscopic examination revealed a rough inside edge of the post hole, as well as "point" contact between the post and the ceramic.

As second sample was fabricated using a revised machining technique to minimize the hole roughness. The posts were placed into the ceramic holes using an epoxy filler to avoid the point contact. Use of the epoxy distributes the load evenly over the edge of the hole. For this sample a torque in excess of 8 in-oz. was reached. This is the maximum calibrated capability of our torque

wrench. We suspect that a considerably higher breakage torque would be measured. A new wrench is being procured.

We plan to perform a finite element analysis of the post/ceramic region to investigate the susceptibility of the ceramic to breakage. We also intend to fabricate posts and connector shells from titanium, rather than the existing aluminum, so that we can expose the tightened samples to hot saline testing.

Analytical Tests on the Glass Seals

During this quarter we performed the first of the analytical tests to be performed on the glass seals and the seal design.

We investigated whether the binding strength is a function of firing temperature. Samples were made by using different maximum firing temperatures and tested for tensile strength on an INSTRON test machine.

(a). For sealing glass B-10041 (vitreous): Softening point: ~343°C,
Firing Temperature: ~370°C.
Seven different firing temperatures were tested: 330, 340, 350, 360, 370, 380, 390 °C.

(b). For sealing glass B-10042 (crystalline): Softening point: ~336°C,
Firing Temperature: ~370-400°C.
Nine different firing temperatures were tested: 320, 330, 340, 350,360, 370, 380, 390, and 400°C.

Code	B-100041	B-100042
Type	Vitreous	Crystalline
Softening Point	343°C	336°C
Annealing Point	289°C	281°C
Crystalline Peak	N/A	491°C
Firing Temperature	370°C	370-400°C

Our initial testing was performed using glass microscope slides. This permitted refining of the sample preparation and testing protocol. We believe that these glass slide tests are relevant to the use of the glass seal with the ceramic since SEM examination of the seals whether on glass or ceramic shows consistent cohesive failure.

Methods:

Green seal material preparation:

The glass powder is a high-purity material with an average particle size smaller than 0.1 micron. A dispensing vehicle was added to the glass powder according to a fixed weight ratio, empirically determined, in order to make a creamy paste-like mixture. The mixture was mixed for about 5 minute in an aluminum container to help break up agglomerates. The mixture was then poured into the reservoir of a 3-cc dispensing syringe.

Dispensing:

A syringe fitted with a small-gauge dispensing tube was controlled by an EFD auto air syringe system. To obtain the required controlled geometry of the seal, a numerically-controlled X-Y table was used to move the syringe over the sample.

Drying:

The green seal were examined by optical microscopy to ensure the topography of the seal track. An oven was used to dry out the moisture and the vehicle from the green seal. Any residue left in the green seal can form voids and holes inside the bulk of the seal during the firing process.

Firing:

A variety of tests were used to determine the temperature range suitable for firing the glass seal. Small glass pieces were sealed on ceramic plates using various firing temperatures. Each sample was examined with an optical microscope to determine whether crystallization had occurred. The temperature at which the glass particles began to spheroidise (due to surface tension) was taken as the lower firing temperature limit, while that where the glass pieces showed visible uniform crystallization on either the surface or in bulk was taken as the upper firing temperature limit.

Each package was fired by placing placed in a open-air atmosphere furnace and heated to 300-400 degree centigrade, with the specific temperature determined by the sample classification. The heating rate was carefully controlled to eliminate the pressure-induced blow-out effect caused by the difference of the air pressure between inside and outside of the package. The main principle of controlling the heating rate is to slow it down sufficiently so that the pressure can equalize before the temperature gets up to the softening point of the glass seal. This method helps to ventilate the air out of the package before the sealing material changes into liquid and seals. We found a heating rate around 2°C/minute to be effective. After the softening point, the heating rate was increased to about 5°C/minute until the temperature reached the desired firing temperature. All packages were kept in the furnace at the highest sintering temperature for at least 30 minutes to improve the homogeneity of the seal. The cooling procedure for all of the packages was identical: After the desired firing temperature was reached, the furnace power was turned off until the temperature of the chamber dropped close to room temperature.

Mechanical Properties Testing

Sample preparation:

After the green glass was mixed, it was dispensed on the surface of substrates. Our initial test specimens consisted of glass microscope slides and were used to refine the testing methods. Duplicate tests, using the Macor ceramic, are now in process.

Ten straight lines (about 1 inch long and 0.02 inch wide) were deposited on the one of each pair of glass slides. The distance between each glass line was 0.04 inch. The green seal was dried and fired. Sintering temperature varied from 350°C to 400°C.

To each sealed pair of glass slides, two aluminum pull-handles were affixed using 2-ton clear epoxy. The pull-handles were subsequently connected to the jaws of the tensile tester.

Tensile Test:

A tensile test, using constant strain rate, was used to evaluate the binding strength of the glass seals. All the tensile tests were carried out at room temperature on an Instron tensile machine (Model 4507). The tensile strain rate was fixed at 5x10E-2 in/min for all samples. The data we obtained from the tensile test are a series of load and displacement pairs. The maximum stress was calculated based on the raw data. To determine the relationship between the firing temperature and the binding strength, seven samples were tested for each firing temperature.

Results:

The mechanical properties requirements for the seals of the hermetic package and feedthroughs are not industry-standardized. There are a variety of implantable electronic packages, used in different applications, and each has different requirements for the mechanical properties of the seal and the package. In this project we have concentrated our efforts on determining the optimal combination of firing time and temperature that results in highest mechanical strength of the seal.

The mechanical property test results, as shown in Fig.3, indicate that the binding strength (psi)of the glass seal increases with the increasing firing temperature over the range of 355°C to 400°C. There is a significant change in maximum stress of the seal when the firing temperature goes from 360°C to 380°C, with the maximum stress increasing from about 600 psi to 900 psi. After 380°C, the maximum stress goes up slowly with increasing firing temperatue. The thin-film metalization that we intend to use on layers #1 and #2 may deteriorate if exposed to firing temperatures in excess of 400°C. Based upon this limit, our criteria for choosing the optimum firing temperature, 385°C, was made on the relationship between the mechanical properties, the metalization limit, and the firing temperature.

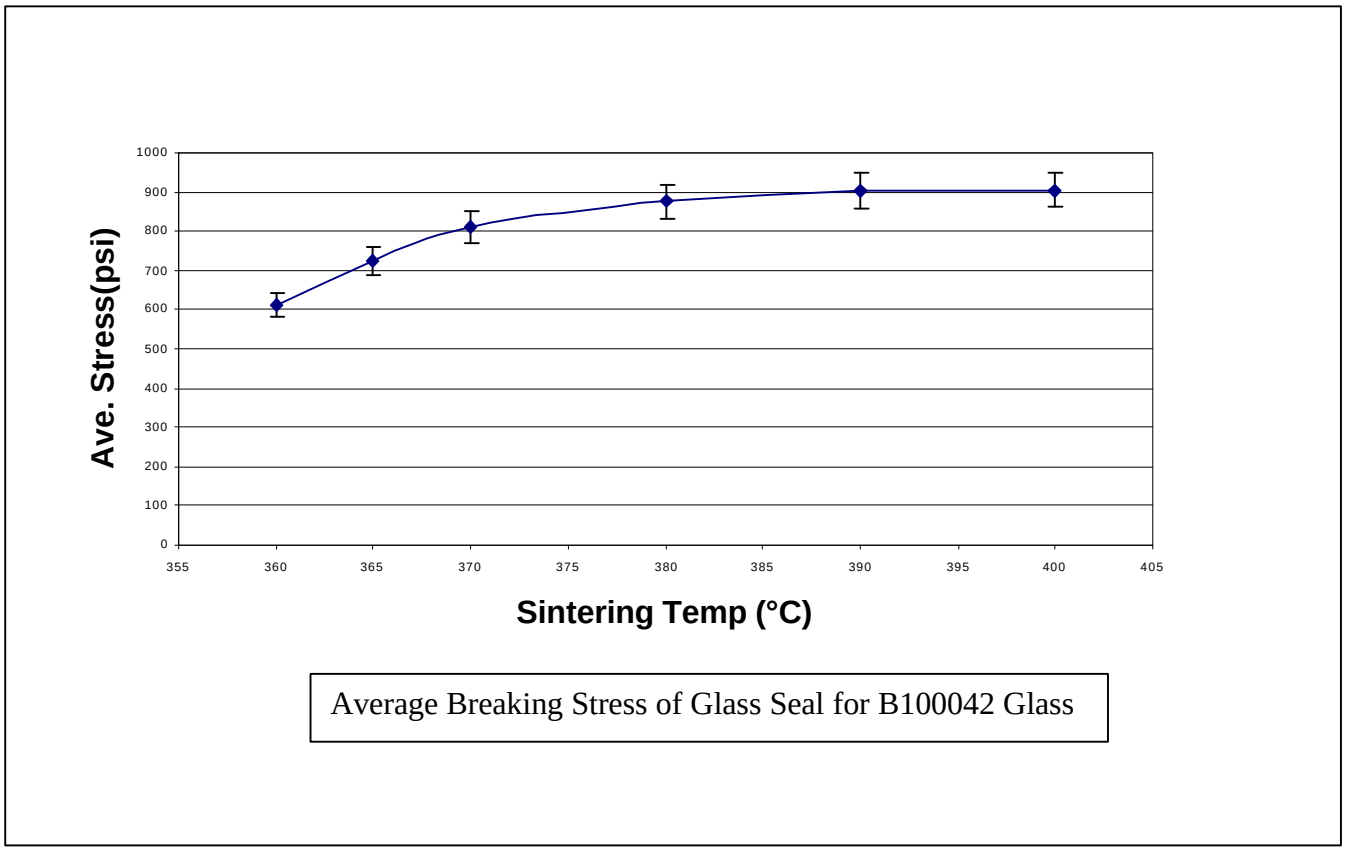


Figure 3 – Tensile Breaking Stress of Glass Seal in PSI

Based upon these results, we have tested a limited number of ceramic-to-ceramic samples. WE find that the bond strength of these samples, fired at 385°C, is significantly higher than those found with the glass samples. The average of our first samples is 1100 psi. We intend to intensify our testing of the ceramic samples during the next quarter.

Progress on the design and fabrication of the submodule ASICs.

During the past quarter we have tested the ASIC, BLOCK3. We designed and submitted for fabrication two new ASICs: FSM1, the first version of the submodule finite state machine, and MOS11, the first version of the front end rectifier and data demodulator. M We have also made progress on designing a microcontroller, connected to a PC for testing, control, and laboratory use of the 8-channel BLOCK chips.

Testing of BLOCK3

During the testing of BLOCK2, we had observed some mismatch between identically designed DACs on the same die. In evaluating BLOCK2, we had found an improvement, over earlier designs, in the anodic-to-cathodic matching. For some DACs the match was as close as 2%. However, for other DACs the mismatch was larger, up to 15%. In order to achieve a wide

compliance voltage range, we used a unique regulation of the current mirror voltages, as described in our earlier reports. We had determined that variations in the offset voltage of the voltage regulators caused by lithographic limitations were responsible for the DAC-to-DAC variations. Our BLOCK3 design, described in our last report, used larger transistors in key circuits in order to minimize the lithographic effects.

In this quarter we implemented a computer-controlled testing system for the BLOCK chips. A graphical user interface was written in LabView that controlled a group of Keithley equipment. This system allows for automatic testing of the BLOCK chips. Detailed measurements of each DAC on each BLOCK chip were made. The biphasic output currents were measured while controlling the output voltage of the DAC from 0 to 10 VDC. The data were automatically collected and formatted in an Excel spreadsheet. Each BLOCK chip requires approximately 23 hours for complete testing. To date we have tested 10 different chips, five of the BLOCK2 design and five of the BLOCK3 design.

Using Excel we analyzed the three types of behavior: the linearity of the DAC, the anodic-to-cathodic matching, and the variation of the output currents for changes in the electrode voltage. The data content and volume are significant, so in this report we present typical data taken from two chips – one of BLOCK2 design, and one of BLOCK3 design. In the next report we will present data that have been compiled from several chips.

Linearity:

A simple plot of the DAC currents vs. current step does not reveal the details concerning the deviations from the DAC currents that would be expected if the DAC were perfectly linear. In order to display the linearity error, we normalized the DAC output current to the DAC most-significant-bit (MSB). Then we computed what the least-significant-bit (LSB) should be based upon the MSB and perfect linearity. At each measured DAC step, we then computed the percent deviation from the ideal computed value. Typical plots of this type can be seen in Figures 4 and 5 for the BLOCK2 and BLOCK3 designs respectively.

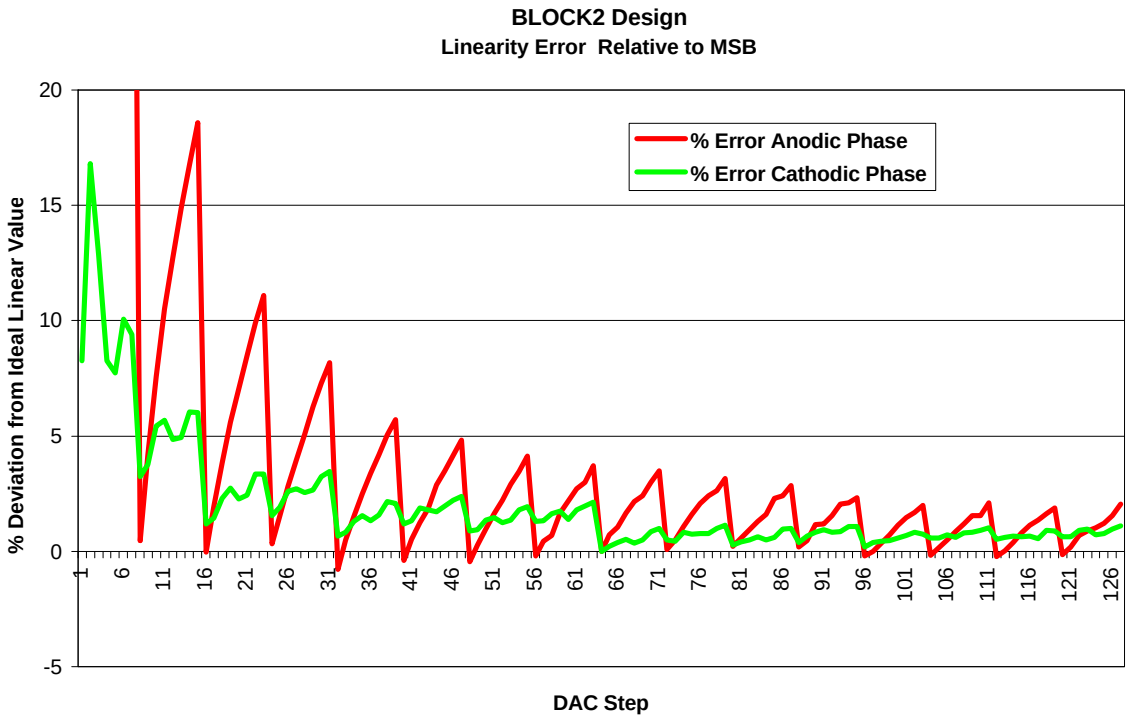


Figure 4 – Linearity Error for BLOCK2 Design

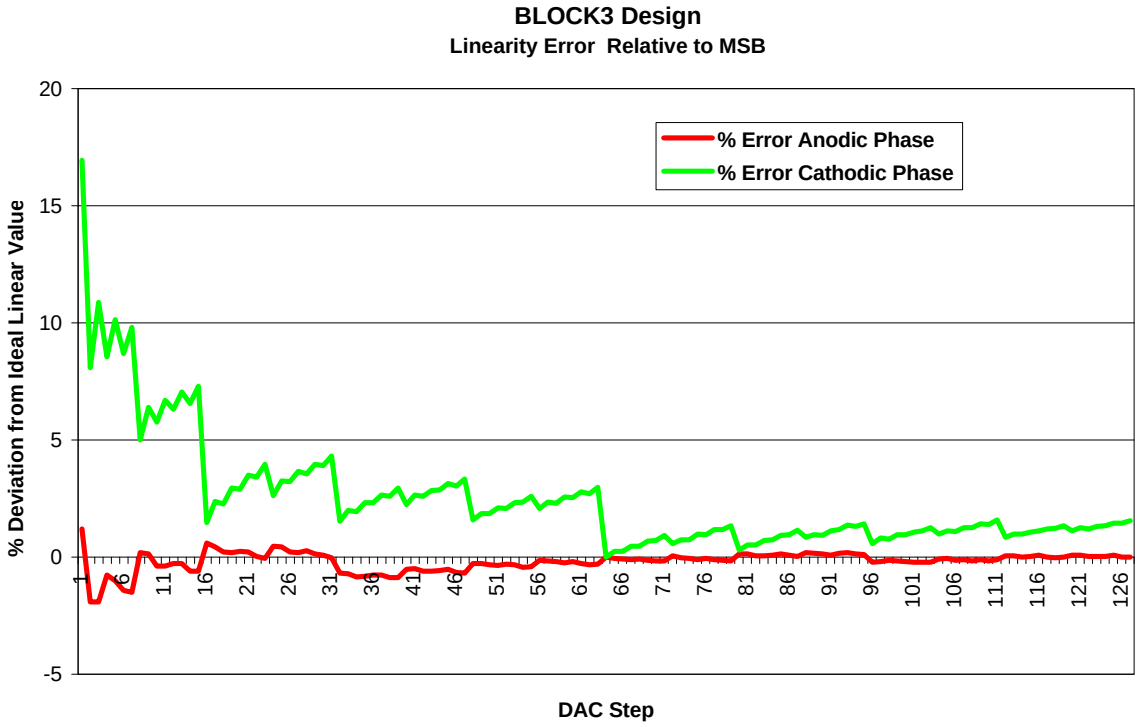


Figure 5 – Linearity Error for BLOCK3 Design

As expected, the error is the worst at the LSB for both designs. However, there is a noticeable improvement in the BLOCK3 design. For the BLOCK2 design the mismatch between the lower 3 bits, and the upper 4 bits is apparent by the repeating error pattern.

Anodic-to-Cathodic Matching:

It is important for the anodic phase to closely match the cathodic phase for each electrode stimulus cycle. In the BLOCK2 design, the topology of the common DAC reference was not able to compensate for mismatches in identically drawn transistors. In the revised BLOCK3 design, the reference was carefully configured to minimize this effect. Figures 6 and 7 show the match between the anodic and cathodic phases for two different DACs, one of BLOCK2 design and one of BLOCK3 design, respectively.

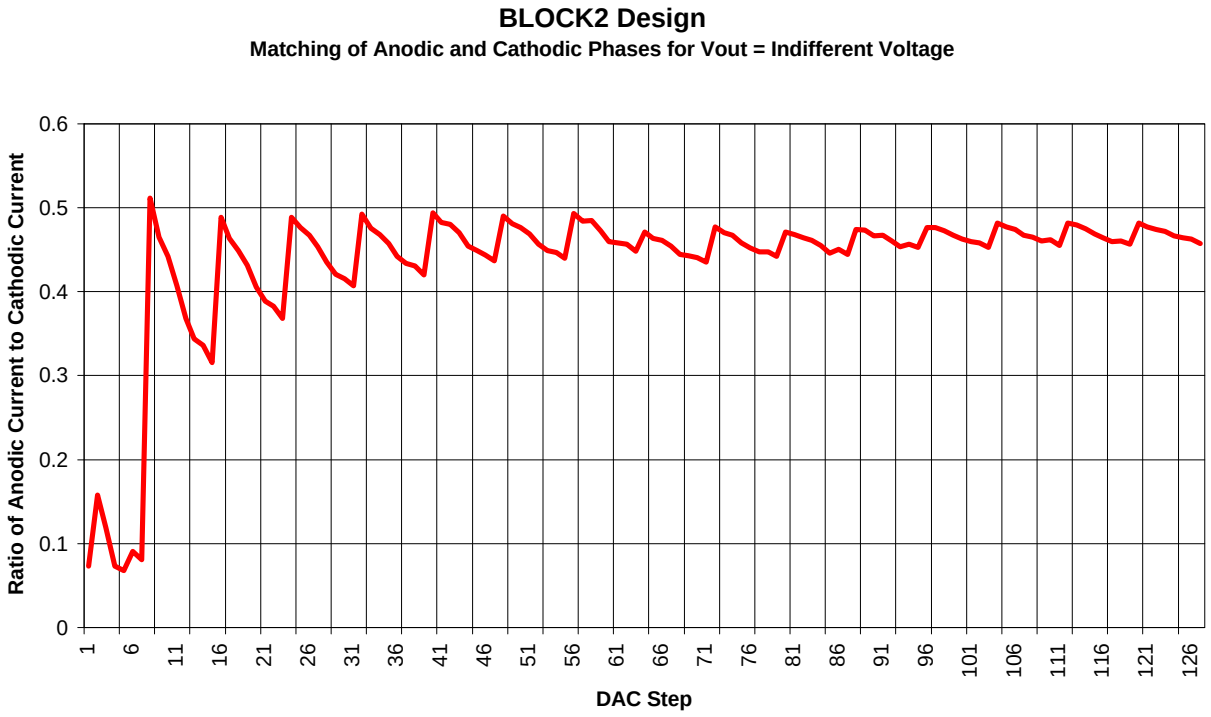


Figure 6 – Matching of Anodic and Cathodic Phases for BLOCK2-type DAC

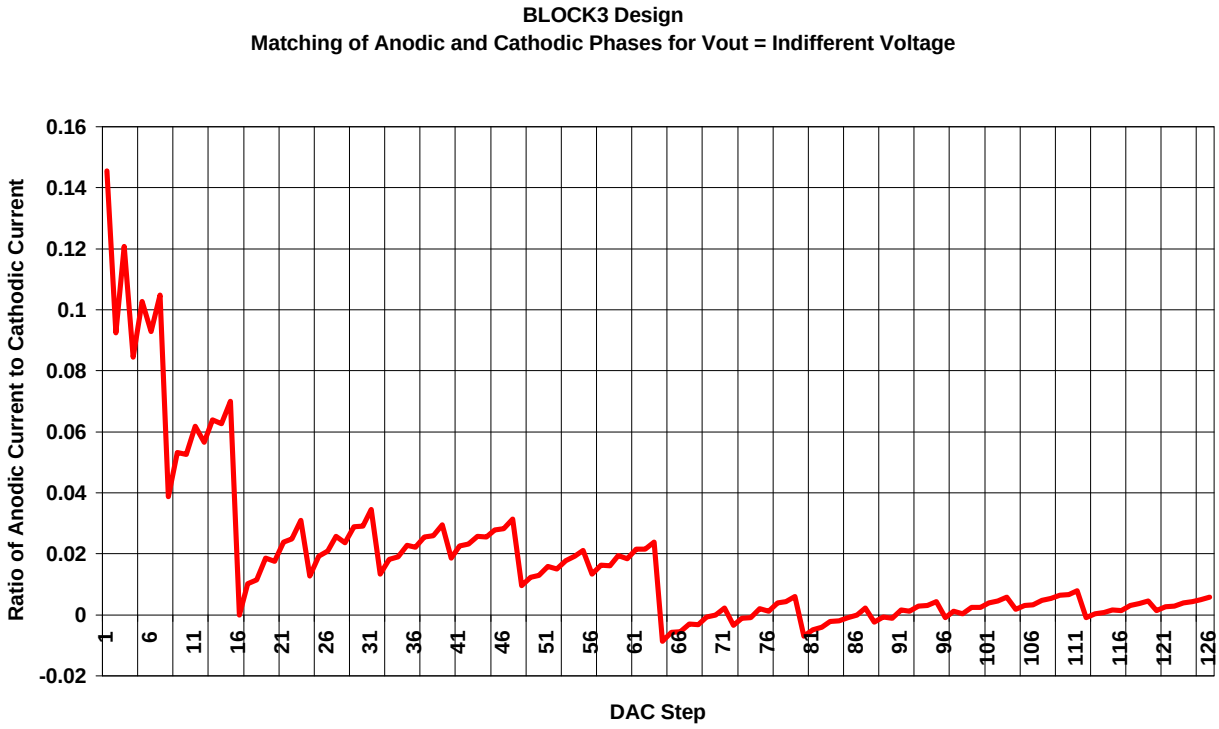


Figure 7 – Matching of Anodic and Cathodic Phases for BLOCK3-type DAC

Note that for the BLOCK2 design, the mismatch between the anodic and cathodic phases is approximately 35% over most of the DAC output range. Whereas for the BLOCK3 design, the mismatch is approximately 2% or less of most of the DAC output range. We are pleased with this lastest design, and when used in conjunction with the electrode coupling capacitor it is likely that this design will preserve the electrochemical integrity of the activated iridium electrodes.

Variations in DAC current for changing voltage:

The variation in the DAC output current with changing DAC output voltage is important for situations in which the electrode capacitance is small. Under this condition, the DAC output voltage can shift towards the extremes of the compliance voltages during the first phase of stimulation. If the DAC cannot maintain constant current for changing output voltage, then a mismatch between the anodic and cathodic phases results. Therefore we tested the variation of the two designs while forcing a change in the DAC output voltage. These plots can be seen in Figures 8 and 9 for the BLOCK2 design and the BLOCK3 design respectively.

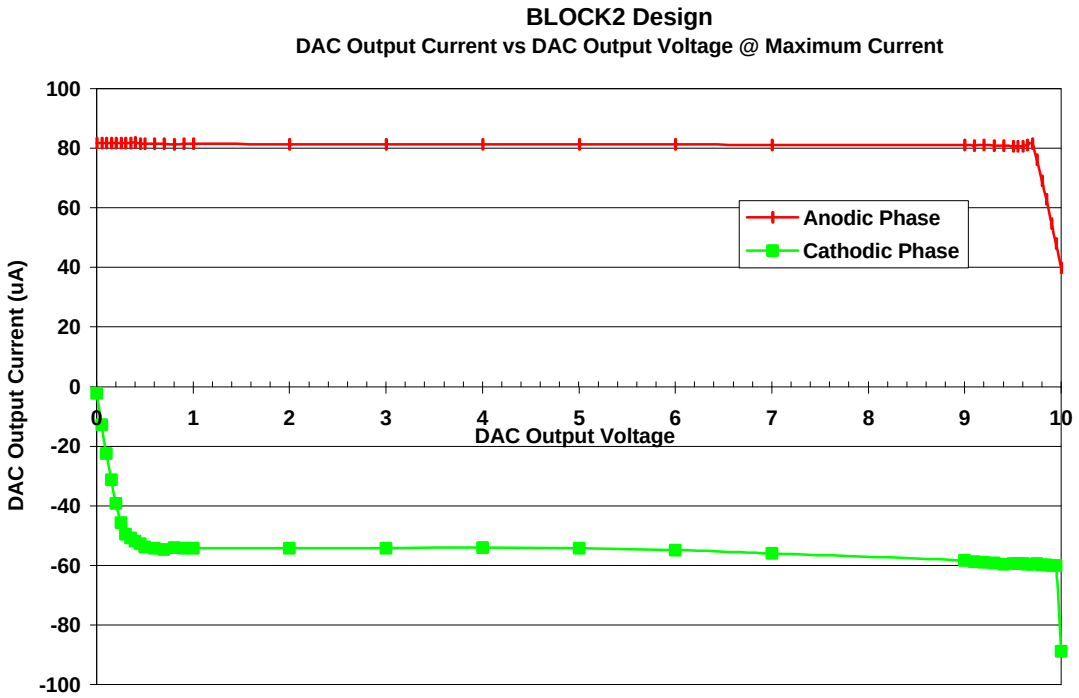
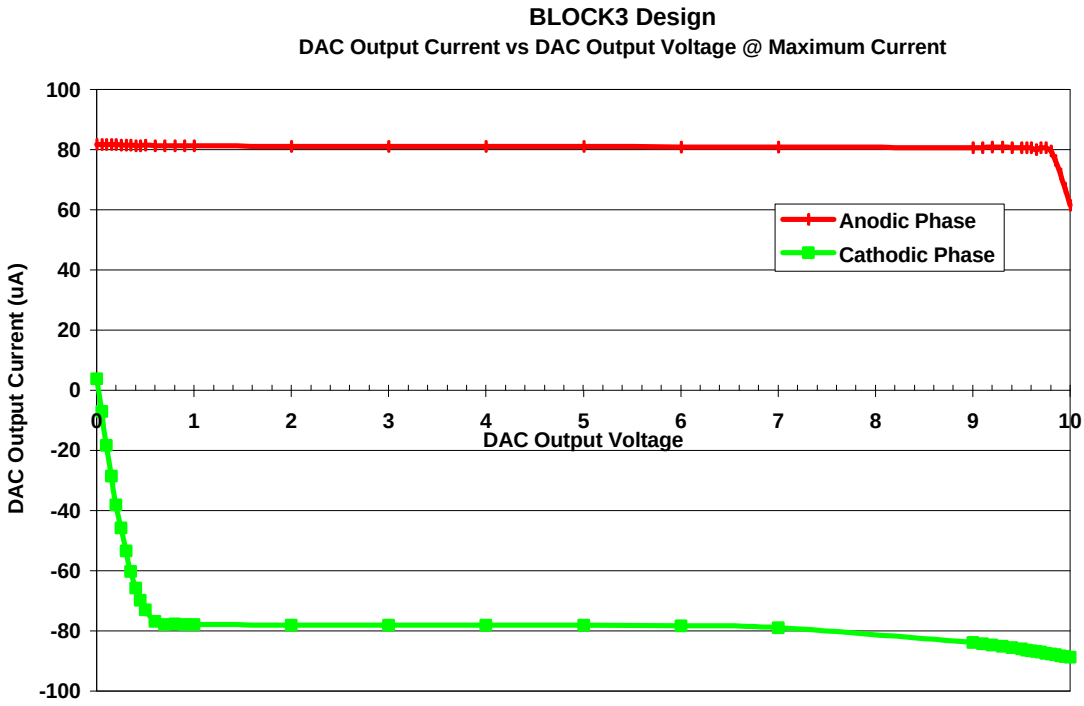


Figure 8 – DAC output current for changing DAC output voltage (BLOCK2 design)



Figutre 9 - DAC output current for changing DAC output voltage (BLOCK3 design)

For both designs, the anodic phase shows a small variation with DAC output voltage and both phases are seen to remain reasonably constant to within 0.5 volts of the compliance supplies. In both the BLOCK2 and BLOCK3 design, the cathodic phase shows a slight increase current as the DAC voltage increases beyond 7 volts. This effect is caused by residual impact ionization current that cannot be corrected by the output stage cascades. It is likely that this current flows directly to the substrate at the drain region of the n-fets used for the current sinks. The current sources, made up of p-fets do not show this effect due to the lower value of impact ionization current that is characteristic of p-fets in and n-well process. Longer n-fets can reduce this effect, however a better solution is probably to use extended drain transistors for the DAC output circuit. We will investigate incorporating the extended drain transistors into a revised design during the next quarter.

Finite State Machine and Front-end Design

During this quarter we designed our first version of the finite state machine (FSM) for control of the submodules. The state machine will decode the digital data sent over the inductive transcutaneous link, and create the necessary digital data streams to control each of the BLOCK chips. We previously reported our adaptation of the SYNOPSIS VHDL simulation and design tool to be compatible with the TANNER layout tools, and this combined tool set was used to design our first generation FSM. This first version does not check parity of the data stream, and does not incorporate the necessary control for reverse telemetry. However, it will provide a complete through-put testing of the implant logic system. This design was submitted to MOSIS and we expect the chips to be delivered by the end of September, 1999. A layout diagram of this chip can be seen in Figure 10, below. On the same MOSIS run, we also placed the first version of the rectifier-front-end chip, shown in Figure 11, below. This chip connects to the implant coil, rectifies the carrier, decodes the suspended-carrier modulation signal and creates a logic-level data stream for the FSM.

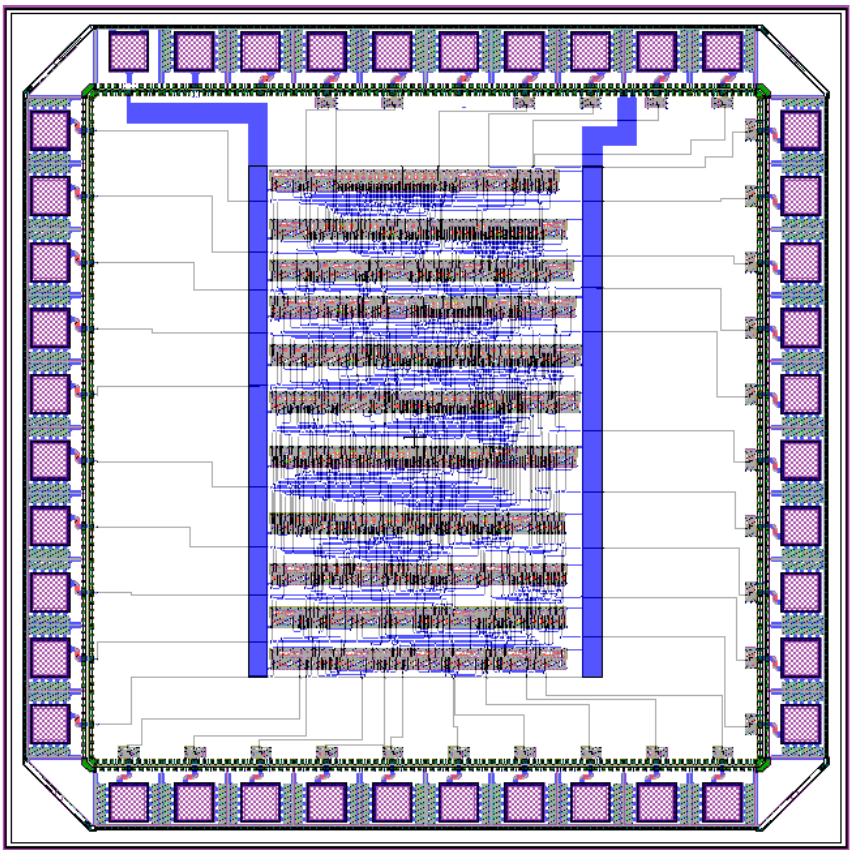


Figure 10 – Version 1 of FSM without parity (size 2mm x 2mm)

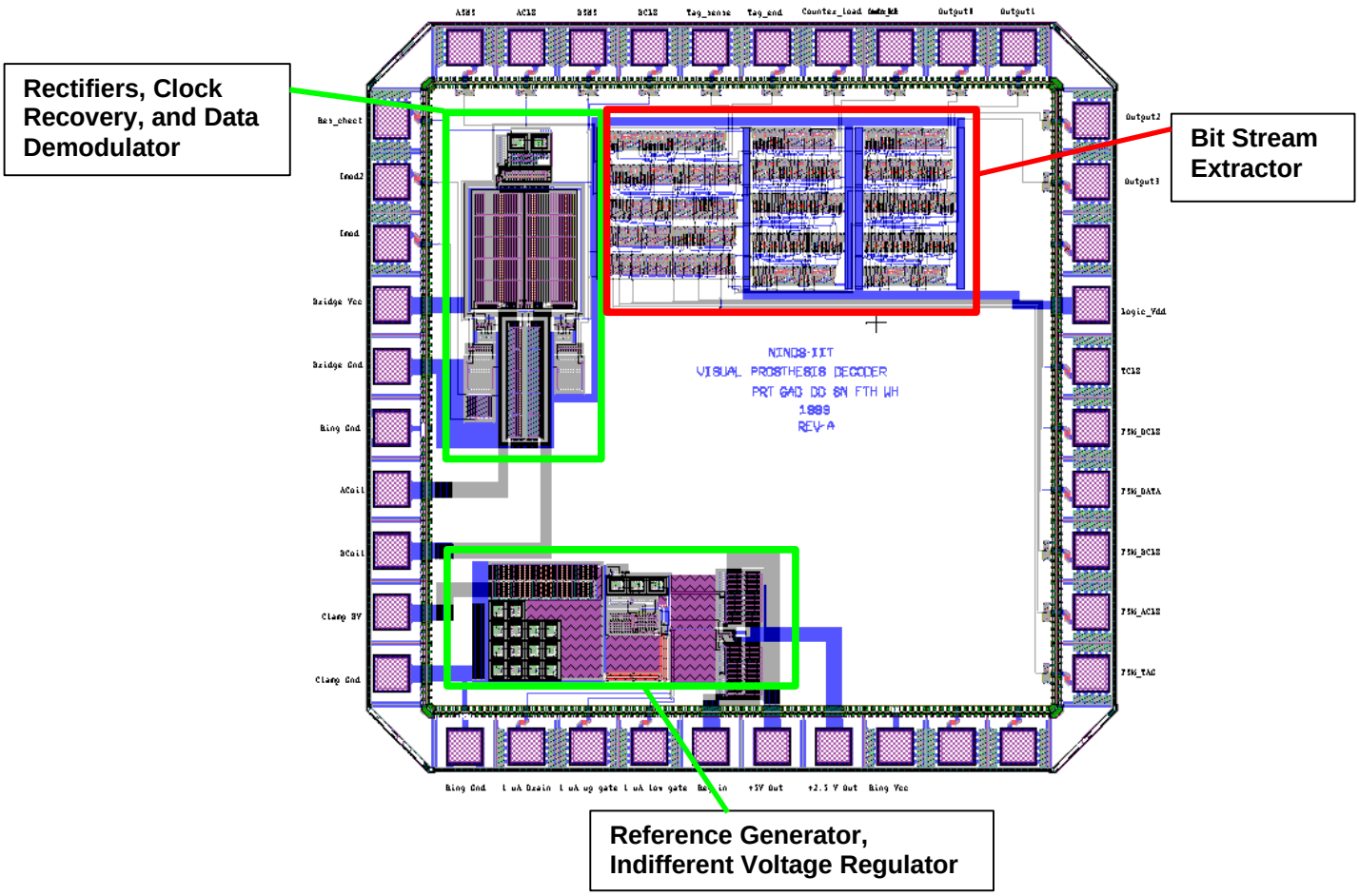


Figure 11 – Version 1 of front-end ASIC for Visual Prosthesis

During the next quarter we plan to test these two ASICs and revise the designs. We also plan to design the version-2 FSM that includes parity checking. We expect that during the next quarter we will be submitting a full wafer run to AMI in conjunction with another project. As part of that wafer run we expect to submit a revised design for the BLOCK chip that contains circuitry for the reverse telemetry measurement of the electrode voltages.